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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,311	01/02/2002	Marvin J. Rich	POU920010005US1	7316

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EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,311	RICH ET AL.	
	Examiner	Art Unit	
	Ayal I. Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18, 10-32, and 34* is/are rejected.

7)☒ Claim(s) *9 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/2/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-34 of U.S. Application 10/038,311 filed on 01/02/2002 are presented for examination.

Specification

2. The disclosure is objected to because of the following informalities: At page 1, lines 13-19, patent application numbers and status are missing. Appropriate correction is required.

Claim Objections

3. Claims 1-34 are objected to because of the following informalities: The preambles of the claims should state the intended use or purpose of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. The prior art used for these rejections is as follows:

6. Balaji, E. et al. "Modeling ASIC Memories in VHDL." Proc. of EURO-DAC '96. Sept. 16-20, 1996. pp.502-508. (Henceforth referred to as "**Balaji**").

7. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

8. **Claims 1-8, 10-32, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Balaji.**

9. In regards to Claim 1, Balaji teaches the following limitations:

1. A method comprising:
storing a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value;

(See Balaji, especially: Sections 6, which teaches that "The tpd_* generics hold the intrinsic delay value pairs. This is passed as a parameter to the PF_Schedule_Output () procedure.")

selecting a rise time delay value and a fall time delay value in a VHDL standard delay file that correspond to an instance of a logic gate in a logic model;

(See Balaji, especially: Sections 6, which teaches that "The tpd_* generics hold the intrinsic delay value pairs ... The following VHDL code in the next page illustrates this implementation ...")

building a rise-time super generic value and a fall-time super generic value for the selected rise time delay value and fall time delay value, the rise-time super generic value representing a rise time delay value stored in the rise time generic variable and the fall-time super generic value representing a fall time delay value stored in the fall time generic variable.

(See Balaji, especially: Sections 5 and 6. Examiner interprets that the claimed "super generic value" corresponds to Balaji's "timing check generics" in the first paragraph of Section 5.)

10. In regards to Claim 2, Balaji teaches the following limitations:

2. The method of claim 1, further comprising:
storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file to represent a rise time delay value and a fall time delay value that correspond to the instance of a logic gate in a logic model.

(See Balaji, especially: Sections 5 and 6)

11. In regards to Claim 3, Balaji teaches the following limitations:

3. The method of claim 2, wherein the rise-time super generic value comprises a pointer to a rise time delay value stored in the rise time generic variable and the falltime super generic value comprises a pointer to a fall time delay value stored in the fall time generic variable.

(See Balaji, especially: Section 4.3, which teaches that "The alternative is to pass the memory as a reference pointer", and Section 5.1 "This is done using a call to PF_Declare_Memory () which returns a pointer to the final memory array.")

12. In regards to Claim 4, Balaji teaches the following limitations:

4. The method of claim 1, further comprising:
repeating the selecting and building steps of claim 1 for every rise time delay value and fall time delay value in the VHDL standard delay file that correspond to every instance of every logic gate in the logic model.

(See Balaji, especially: Sections 5 and 6)

13. In regards to Claim 5, Balaji teaches the following limitations:

5. The method of claim 4, further comprising the step of:
storing every built rise-time super generic value and fall-time super generic value.

(See Balaji, especially: Sections 5 and 6)

14. In regards to Claim 6, Balaji teaches the following limitations:

6. The method of claim 5, wherein the storing step comprises the step of:
storing every built rise-time super generic value and fall-time super generic value in a VHDL standard delay file.

(See Balaji, especially: Sections 5 and 6)

15. In regards to Claim 7, Balaji teaches the following limitations:

7. The method of claim 5, wherein the collective stored every built rise-time super generic value and fall-time super generic value is a reduced storage size than the collective every rise time delay value and fall time delay value from the VHDL standard delay file.

(See Balaji, especially: Sections 5 and 6)

16. In regards to Claim 8, Balaji teaches the following limitations:

8. A method comprising:
extracting correlation delays from a VHDL standard delay file analysis file;
generating a VHDL associative array structure; and

outputting a correlation VHDL file.

(See Balaji, especially: Sections 7, which teaches: "Input edge specifiers are required in generic names. Given below is the SDF construct and the corresponding generics in the VITAL memory model for the above timing arc specifications."

In addition, Sections 6 teaches that "The tpd_* generics hold the intrinsic delay value pairs ... The following VHDL code in the next page illustrates this implementation ...")

17. In regards to Claim 10, Balaji teaches the following limitations:

10. The method of claim 8, wherein the correlation VHDL file comprises a VHDL package file embedded with correlation delay data.

(See Balaji, especially: Sections 5 and 6)

18. In regards to Claim 11, Balaji teaches the following limitations:

11. An apparatus comprising:
a controller/processor;

(See Balaji, especially: Sections 1 "Introduction". The use of a computer with a processor is inherent when modeling using VHDL or Verilog, which are programming languages.)

a data memory for storing a VHDL standard delay file and a rise time generic variable and a fall time generic variable, the rise time generic variable comprising at least one rise time delay value and the fall time generic variable comprising at least one fall time delay value;

(See Balaji, especially: Sections 6, which teaches that "The tpd_* generics hold the intrinsic delay value pairs. This is passed as a parameter to the PF_Schedule_Output () procedure. ... The following VHDL code in the next page illustrates this implementation ...")

a program memory storing an SDF reducer, the program memory communicatively coupled to controller/processor and the data memory, for selecting a rise time delay value and a fall time delay value in a VHDL standard delay file that correspond to an instance of a logic gate in a logic model, and for building a rise time super generic value and a fall-time super generic value for the selected rise time delay value and fall time delay value, the rise-time super generic value representing a rise time delay value stored in the rise time generic variable and the fall-time super generic value representing a fall time delay value stored in the fall time generic variable.

(See Balaji, especially: Sections 5 and 6. Examiner interprets that the claimed "super generic value" corresponds to Balaji's "timing check generics" in the first paragraph of Section 5.)

19. In regards to Claim 12, Balaji teaches the following limitations:

12. The apparatus of claim 11, wherein the SDF reducer stored in the program memory for storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file in the data memory to represent a rise time delay value and a fall time delay value that correspond to the instance of a logic gate in a logic model.

(See Balaji, especially: Sections 5 and 6)

20. In regards to Claim 13, Balaji teaches the following limitations:

13. The apparatus of claim 12, wherein the rise-time super generic value comprises a pointer to a rise time delay value stored in the rise time generic variable and the fall-time super generic value comprises a pointer to a fall time delay value stored in the fall time generic variable.

(See Balaji, especially: Section 4.3, which teaches that "The alternative is to pass the memory as a reference pointer", and Section 5.1 "This is done using a call to PF_Declare_Memory () which returns a pointer to the final memory array.")

21. In regards to Claim 14, Balaji teaches the following limitations:

14. The apparatus of claim 11, wherein the SDF reducer, stored in the program memory, for storing the rise-time super generic value and fall-time super generic value in a VHDL standard delay file in the data memory to represent all rise time delay values and fall time delay values that correspond to each instance of every logic gate in a logic model.

(See Balaji, especially: Sections 5 and 6)

22. In regards to Claim 15, Balaji teaches the following limitations:

15. The apparatus of claim 14, wherein the reduced standard delay file comprises at most, two generics per logic gate instance.

(See Balaji, especially: Sections 5 and 6)

23. In regards to Claim 16, Balaji teaches the following limitations:

16. The apparatus of claim 11, further comprising:

a VHDL correlation generator, stored in the program memory, for extracting correlation delays from the VHDL standard delay file analysis file, generating a VHDL associative array structure, and outputting a correlation VHDL file; and

(See Balaji, especially: Sections 5 and 6)

a VHDL correlation file, communicatively coupled to the VHDL correlation generator.

(See Balaji, especially: Sections 5 and 6)

24. In regards to Claim 17, Balaji teaches the following limitations:

17. The apparatus of claim 16, wherein the VHDL correlation file comprises a VHDL package file embedded with correlation delay data.

(See Balaji, especially: Sections 5 and 6)

25. Claims 18-32 and 34 are rejected based on the same reasoning as claims 1-8 and 10-17, *supra*.

26. Claims 18-24 are system claims that recite limitations equivalent to the limitations recited in apparatus claims 11-17.

27. Claims 25-32 and 34 are computer readable medium claims that recite limitations equivalent to the limitations recited in method claims 1-8 and 10.

Allowable Subject Matter

28. Claims 9 and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims.

29. In regards to Claim 9,

> 9. The method of claim 8, wherein the VHDL associative array structure is a three dimensional data structure comprising:
> a z-axis of the data structure representing a set of common blocks for each logical topology of a VHDL logic gate;
> an x-axis of the data structure representing a delay name for the gate topology; and
> a y-axis of the data structure representing an actual delay value.

Balaji teaches (see p.507, right column, last paragraph) an SDF construct in the VITAL memory model for timing arc specifications. The "Example" in Balaji's

construct appears to have sets of three parameters [i.e. (1:2:3), (4:5:6) ... etc.], however, Balaji does not expressly teach that these sets of three parameters correspond to the x, y, and z-axes claimed in applicants' claim 9.

30. Claim 33 is a computer readable medium claims that recite limitations equivalent to the limitations recited in method claim 9.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (571) 273- 8300, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

August 1, 2005

LEO PICARD
SUPERVISORY PATENT EXAMINER
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